



Innovations in Testing for Truly Known Good High Bandwidth Memory Stacks



Alan Liao - FormFactor
Hiromitsu Takasu - ADVANTEST

High Bandwidth Memory Market Size & Kown Good Die/Stack Test Demands

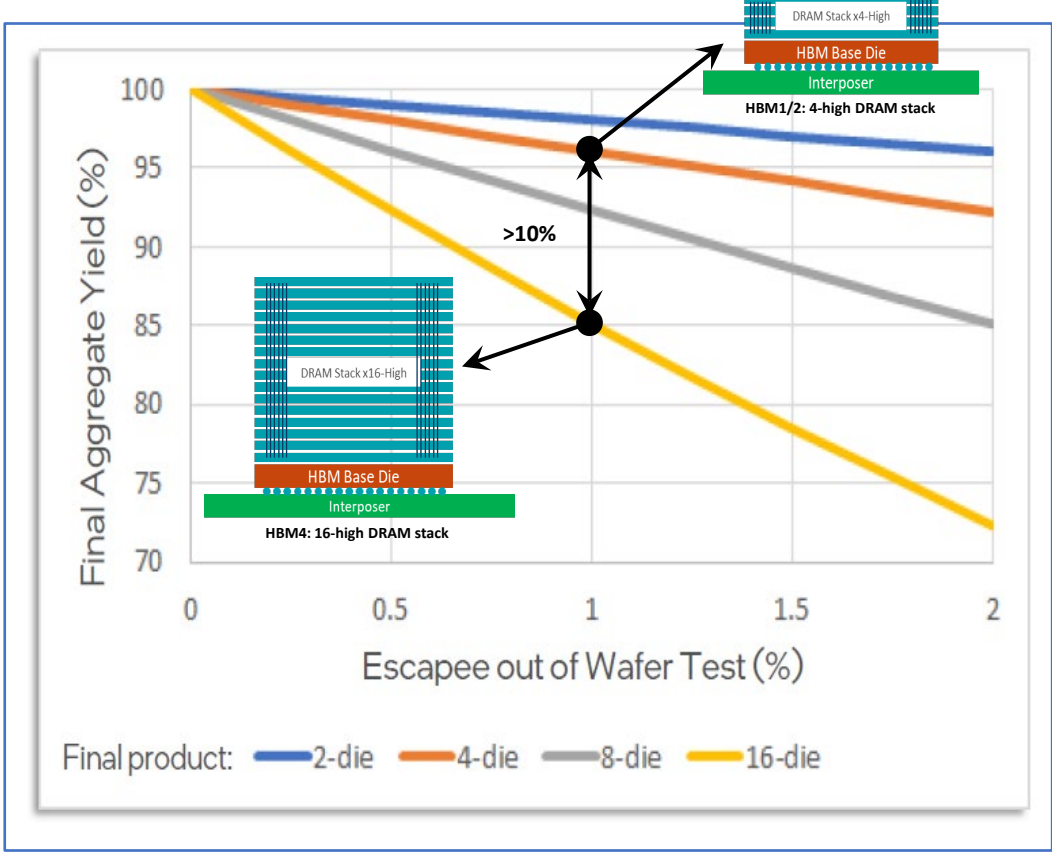
HBM Market Size

- Revenue CAGR 23 ~ 29 at 38%
- Wafer Production 23 ~ 29 at 23%

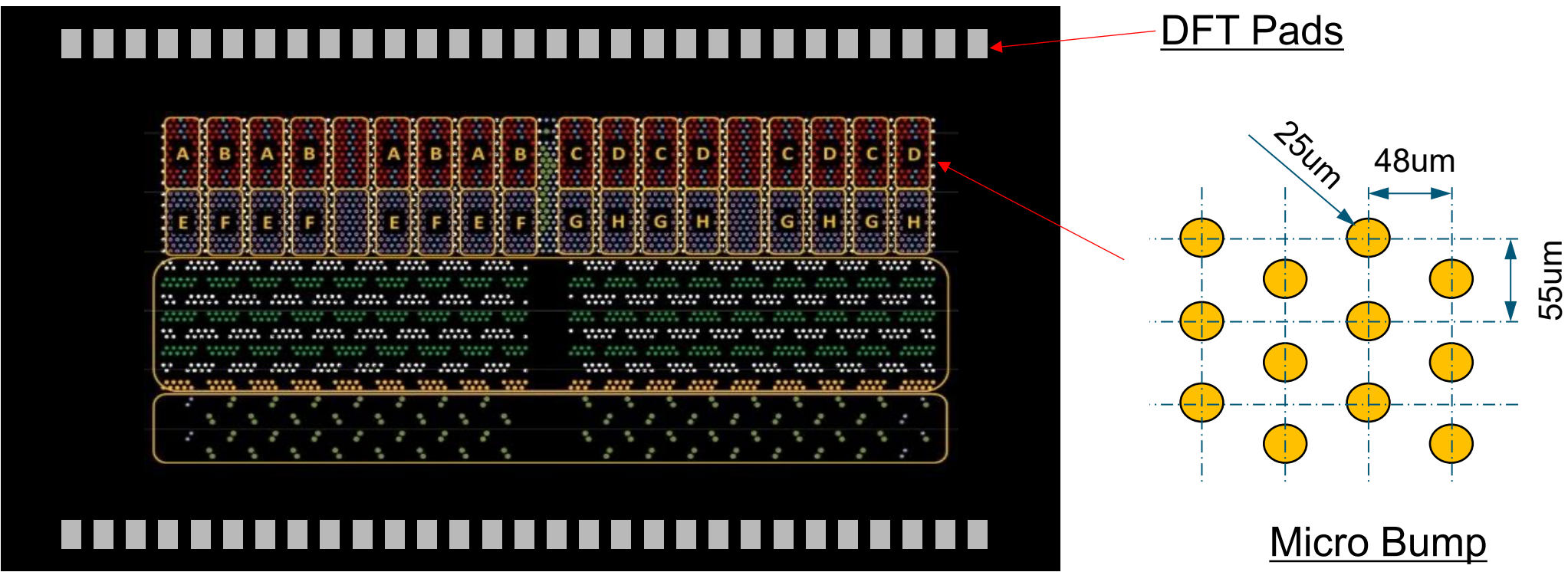
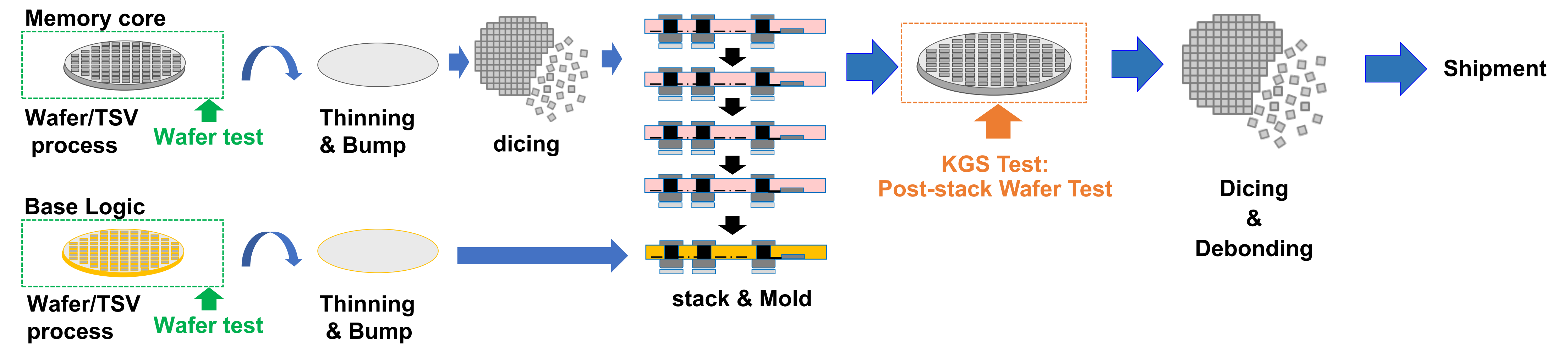
Package final test is necessary, but provides limited insight to improve performance & yield Ideally, each component is good before integration

- Nirvana is Known Good Die (KGD), just test everything
- Economics may dictate something shy of KGD
- Pre-package wafer test → scrap-cost avoidance
- Final-test and system-test opportunities prevent escapes

HBM MARKET FORECAST – OVERVIEW
Source: Next-Generation DRAM 2025 report, Yole Group

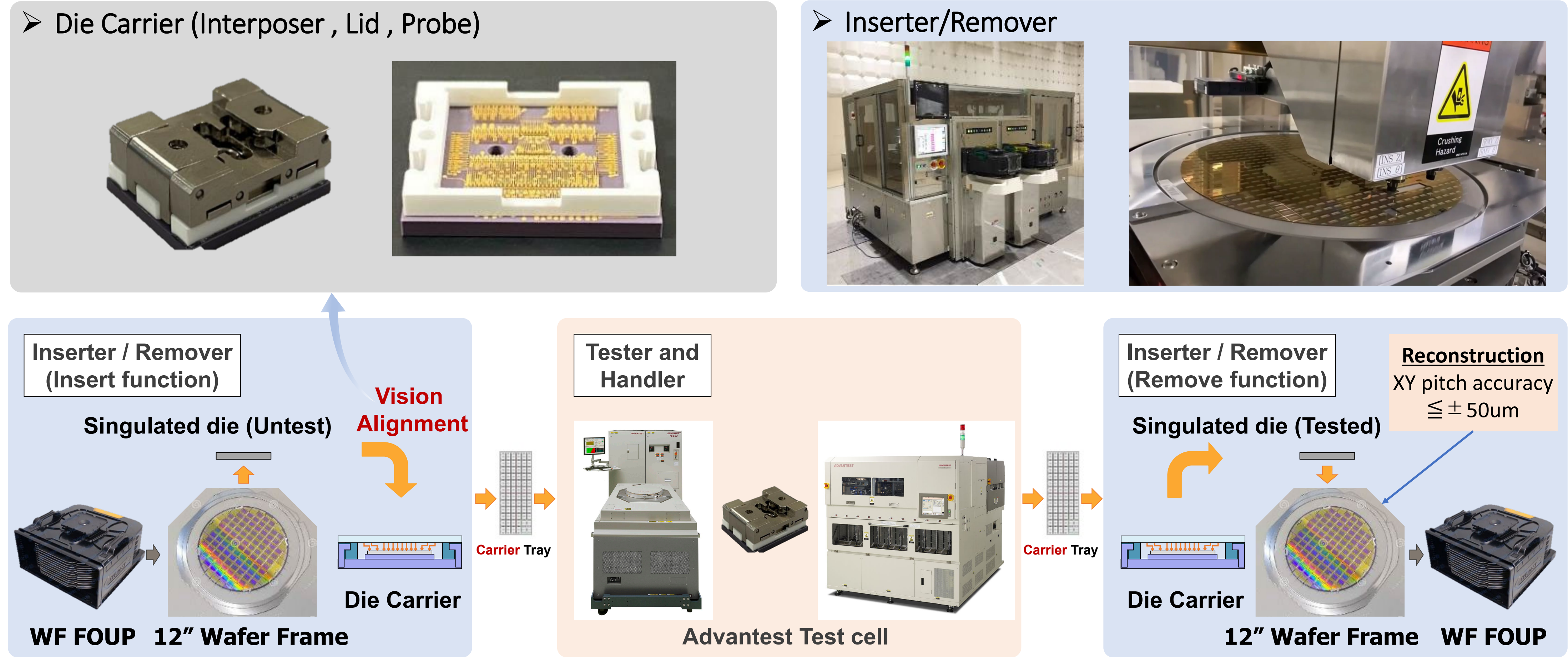


Typical HBM Test Insertion – Pros & Cons on KGD PAD Testing



	Micro-bump probing test	DFT pad probing test
Pros	All 8ch simultaneously test can be executed. Test close to actual usage conditions	Do not damage Micro-bumps. Big number of parallel test can be executed.
Cons	Deep bump coining unusable in production. Small number of parallel test due to many I/O pins.	Test different from actual usage conditions

HBM test cell solution by “Die Carrier”



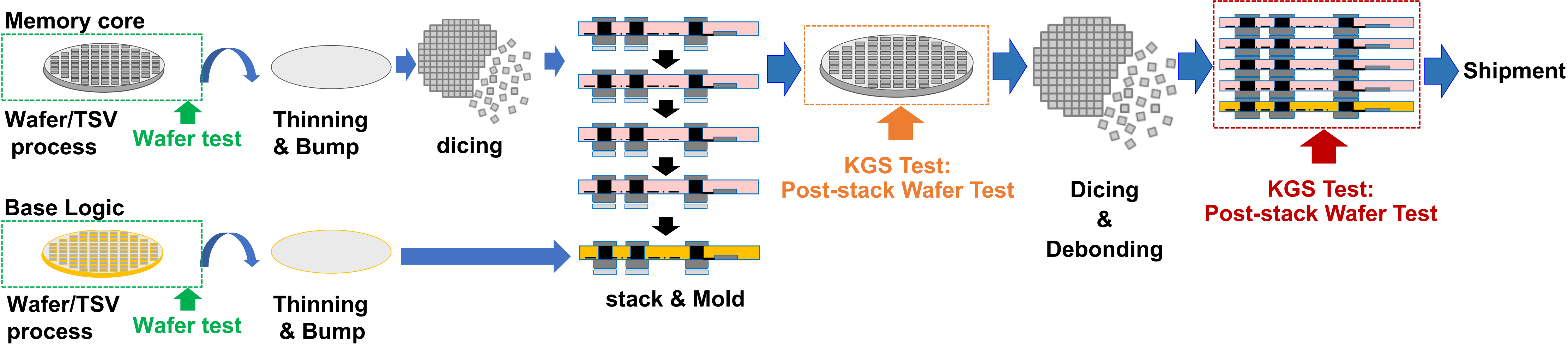
FFI HBM Singulated Stack Die Test Solution

Product Features:

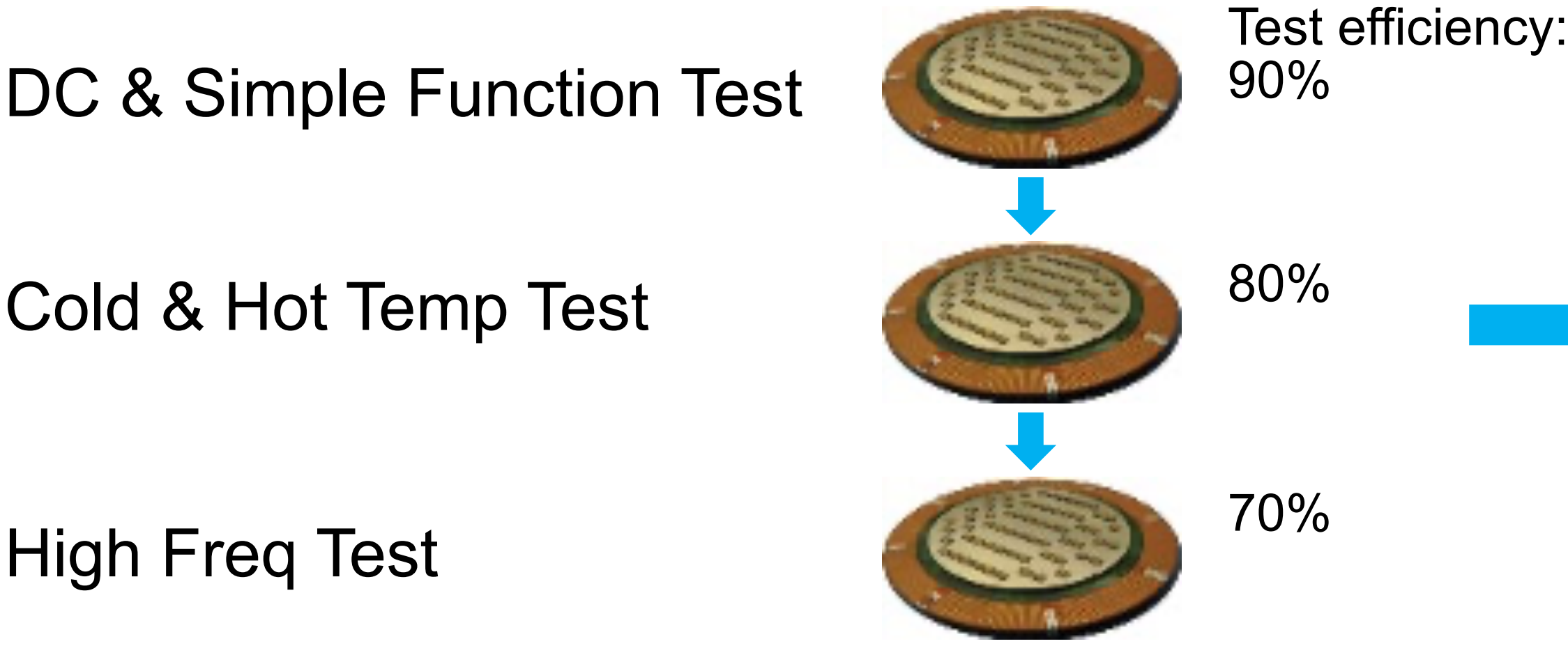
- Compatible with T11 series probe
- Offer same high-speed performance as HFTAP
- Cold and Hot temperature capability
- Design with Advantest handler and tester build in vision alignment feature

Product Benefits:

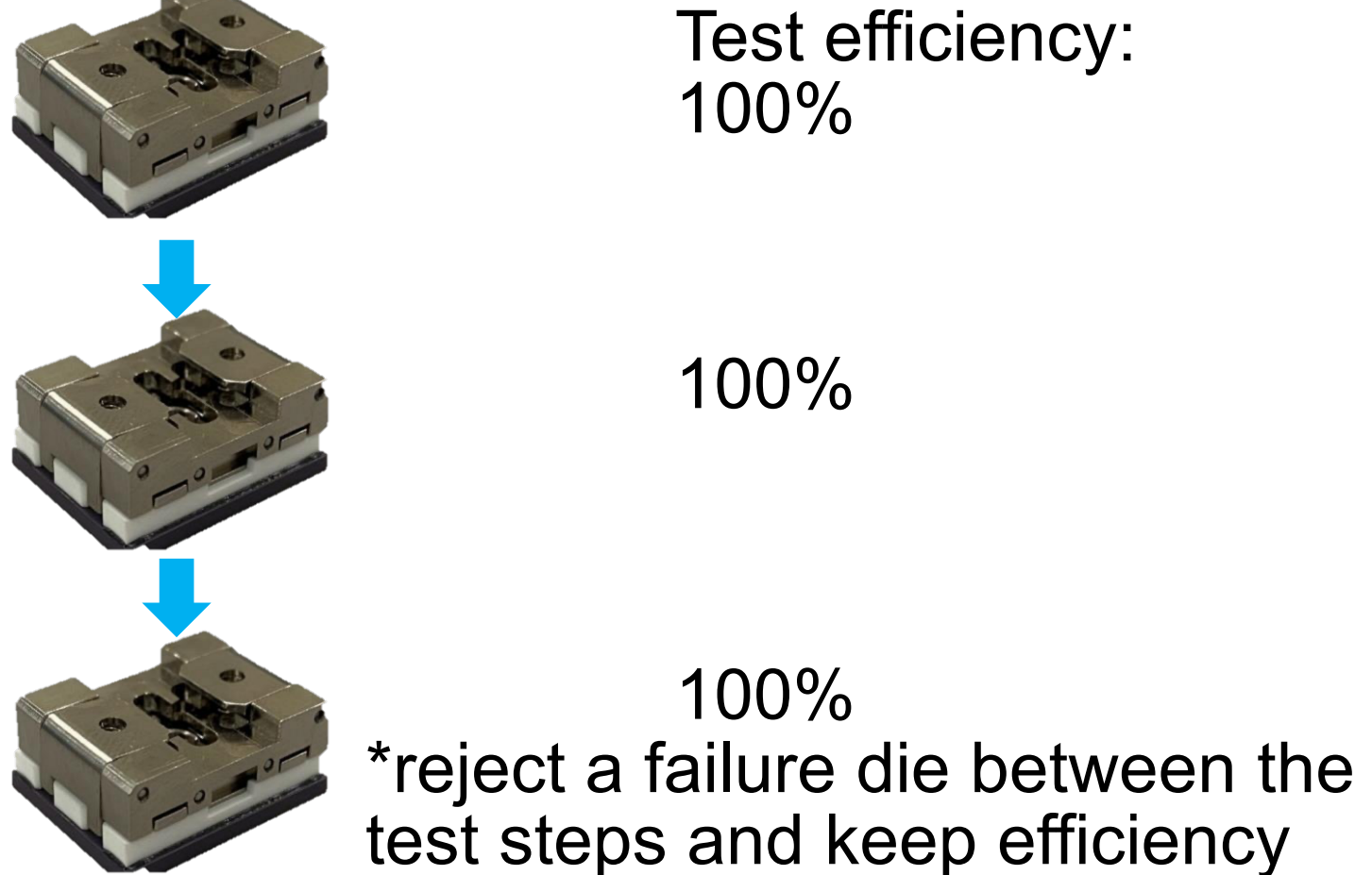
- Offer solution for **truly** known good stack/die test solution
- Enable quality screening post HBM stack wafer dicing
- HBM KGD test capability up to 4GHz
- Fast soak time switching temperature



Known Good Stack Wafer Test Flow



Known Good Stack Die Test Flow



Carrier structure and SI/PI Simulation result

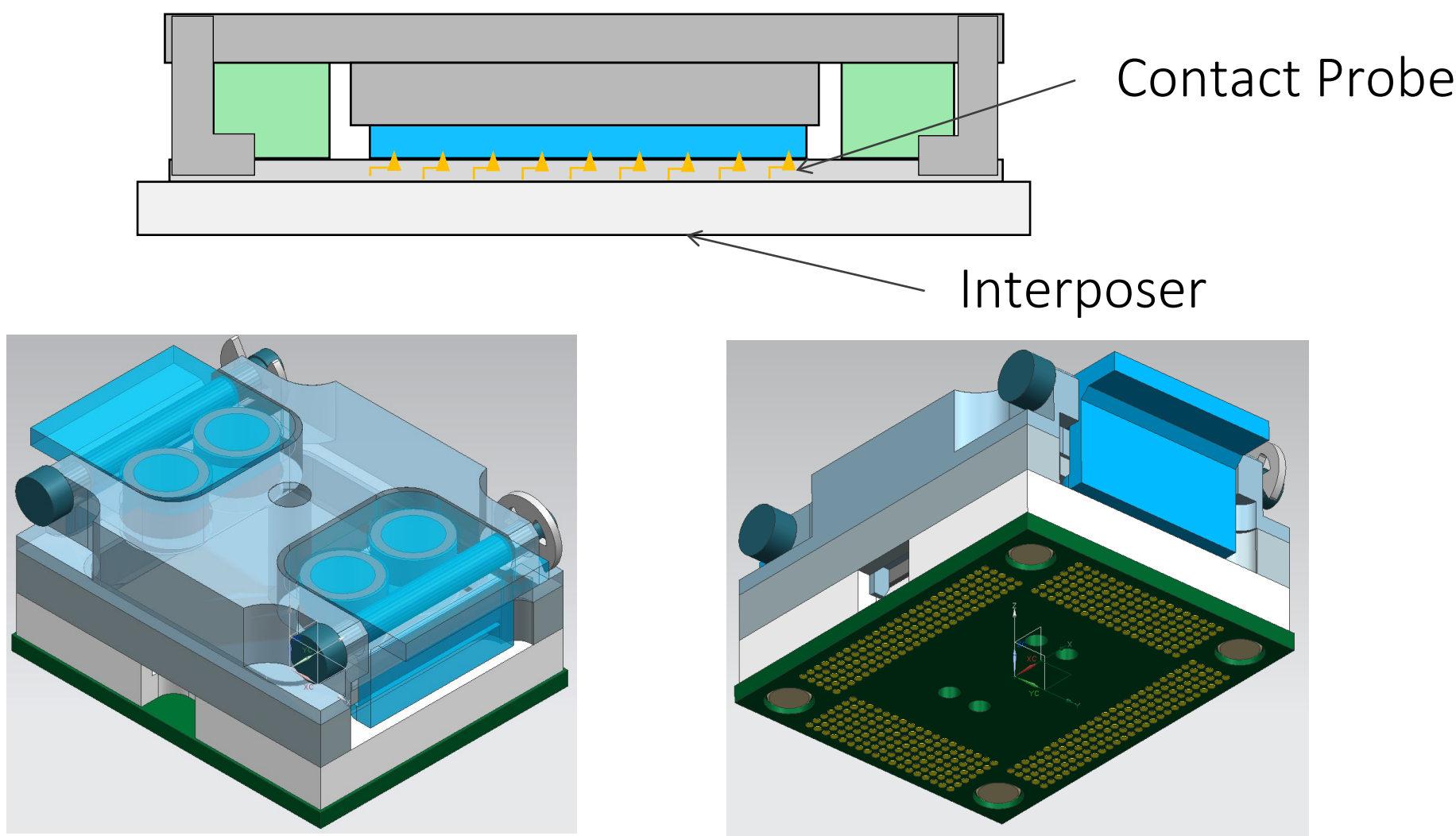
Carrier structure

Structure

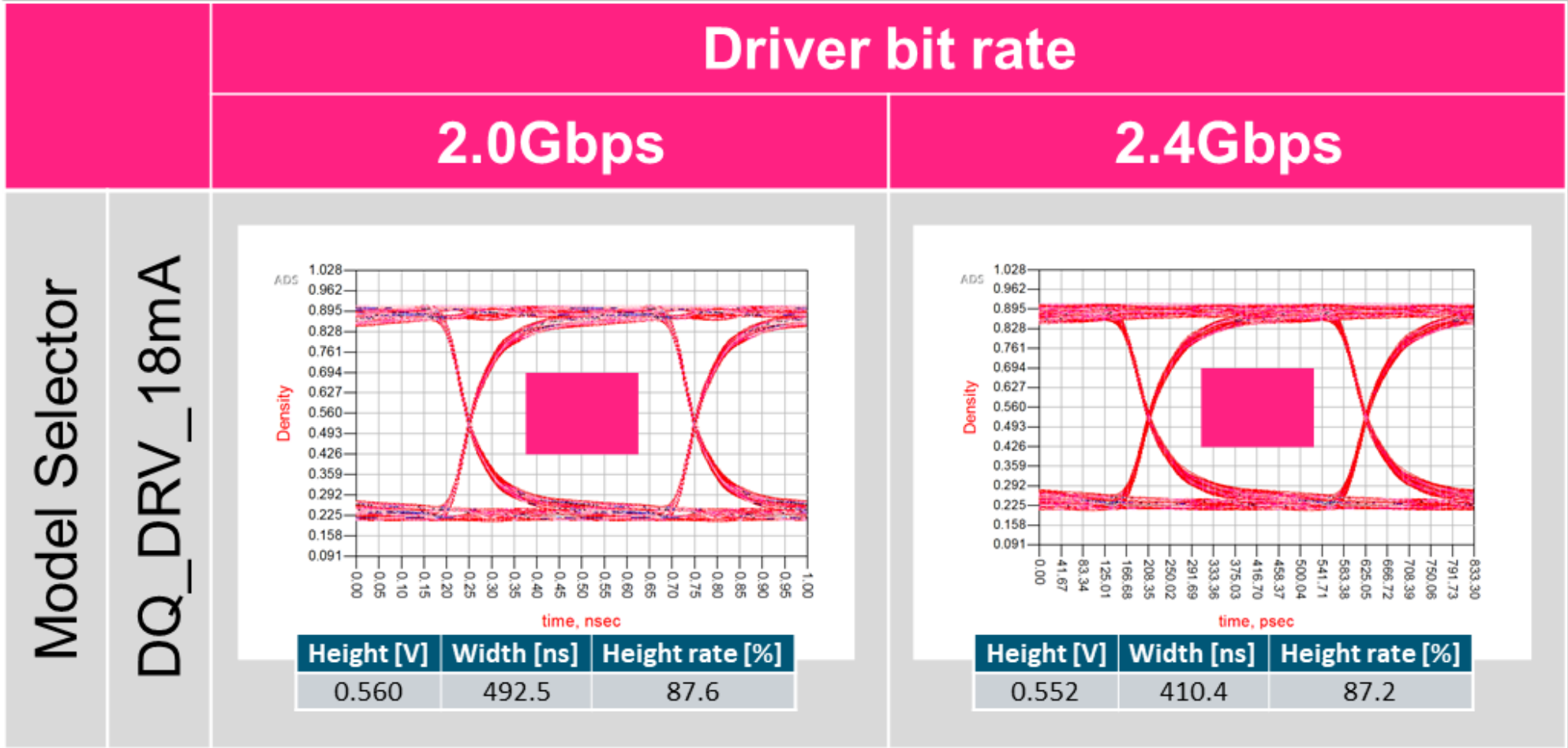
- Contact to HBM device : MEMS Probe
- Contact to test socket : Interposer

Pros

- High electrical performance can be expected
- Similar pad scrub behavior with wafer test

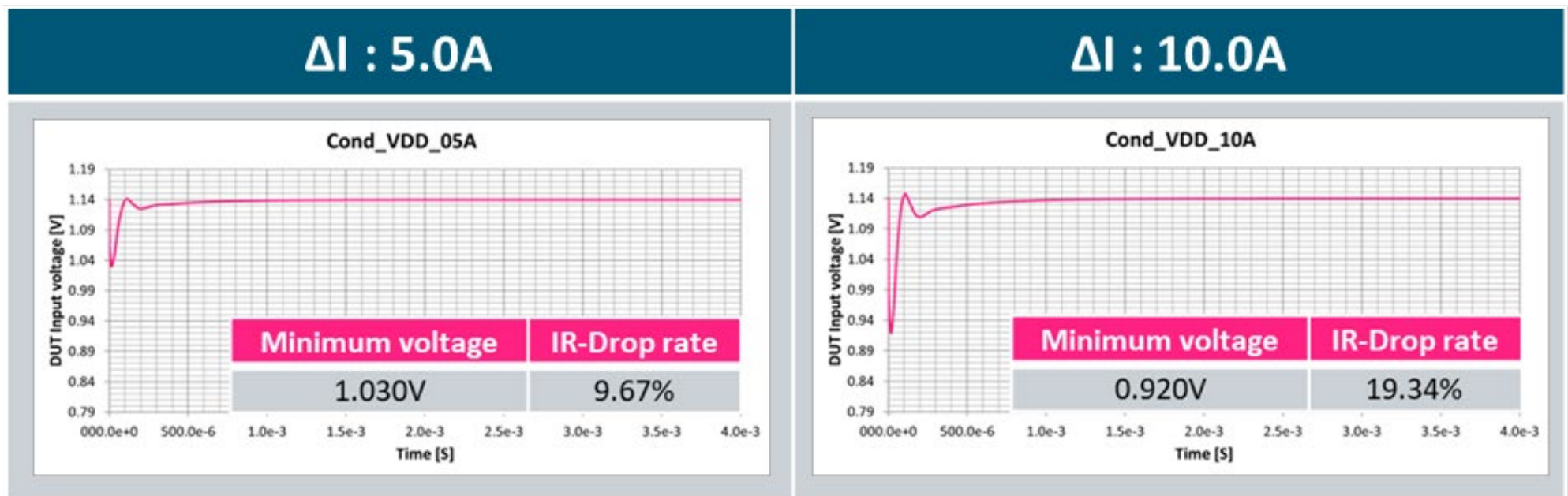


SI Simulation result



T5833 Read cycle simulation results on Carrier Solution

PI Simulation result

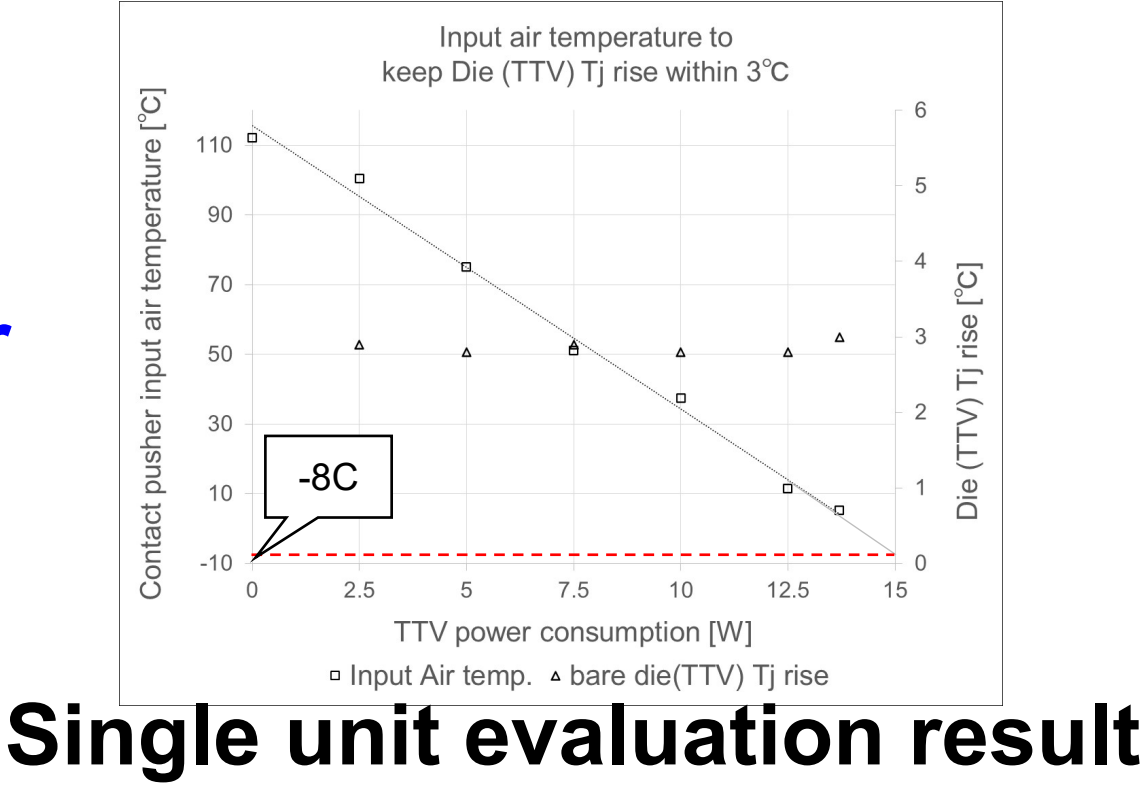
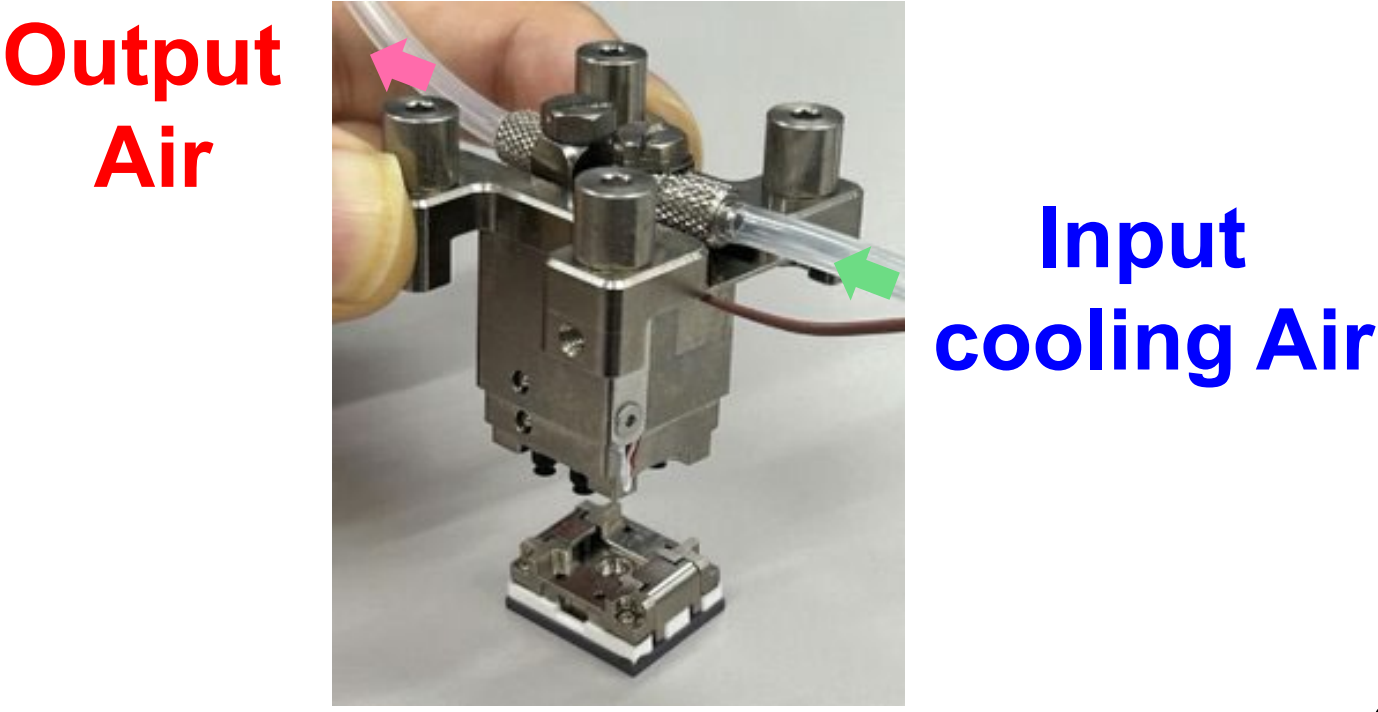


T5833 Power supply simulation (IR-Drop) results

Thermal technical challenge

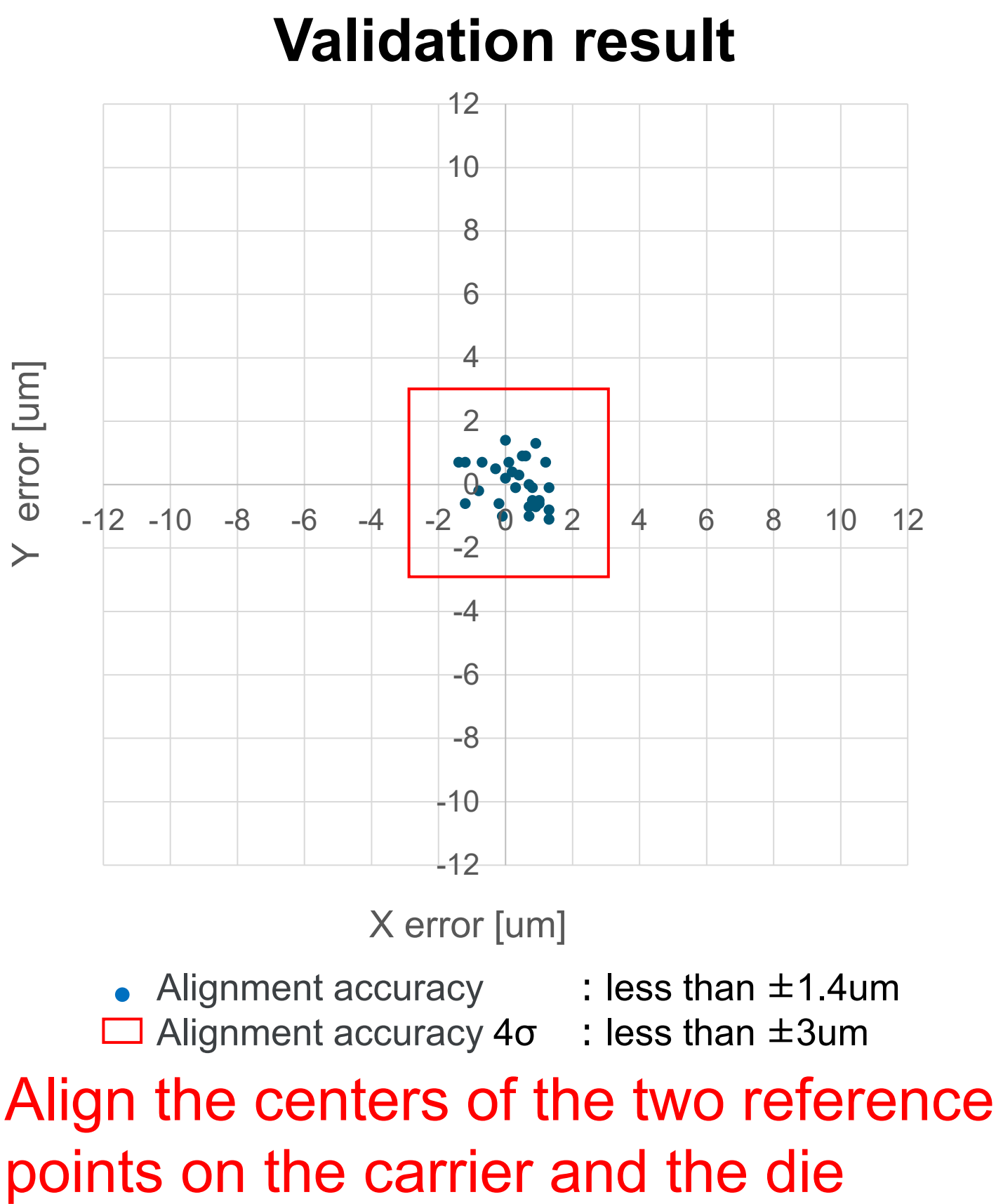
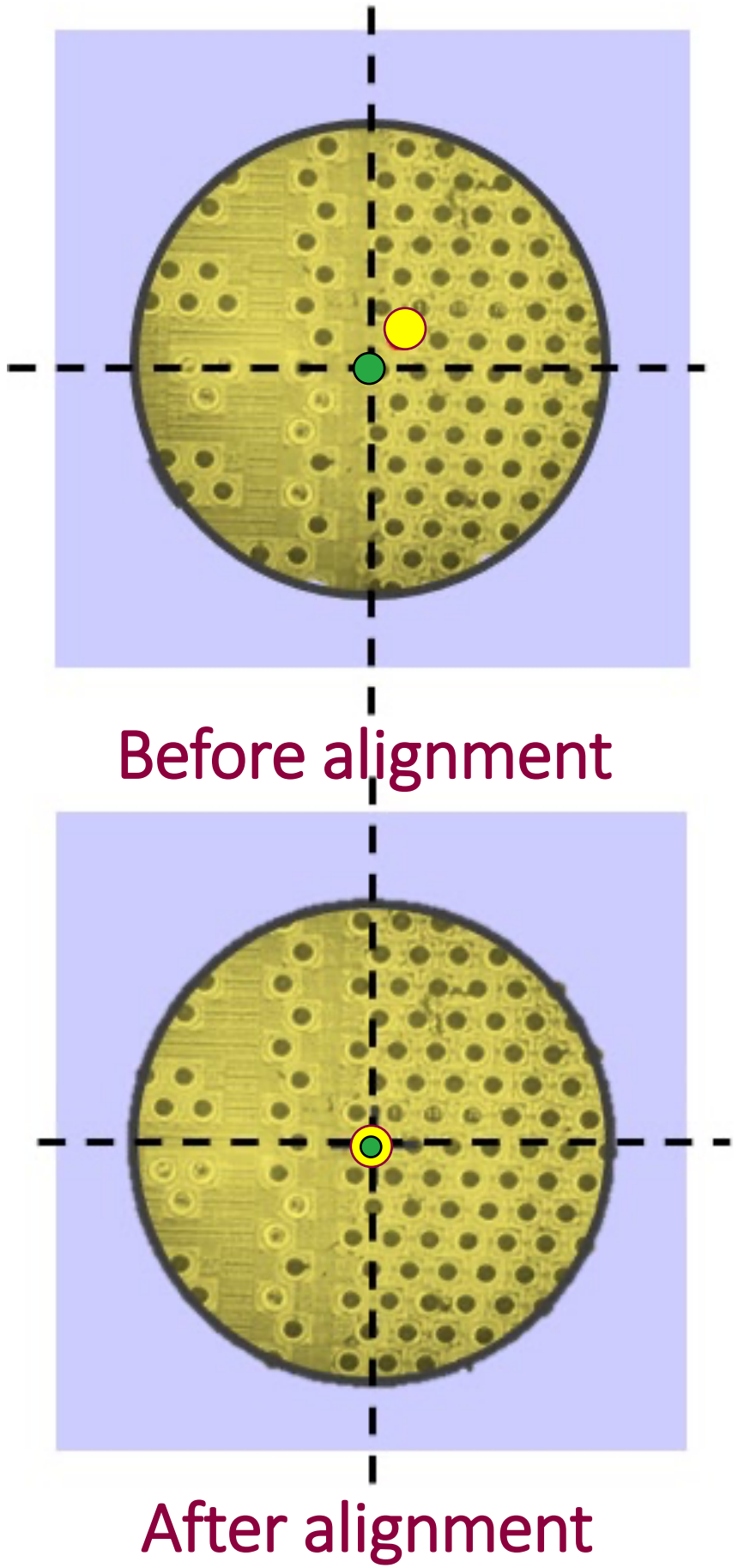
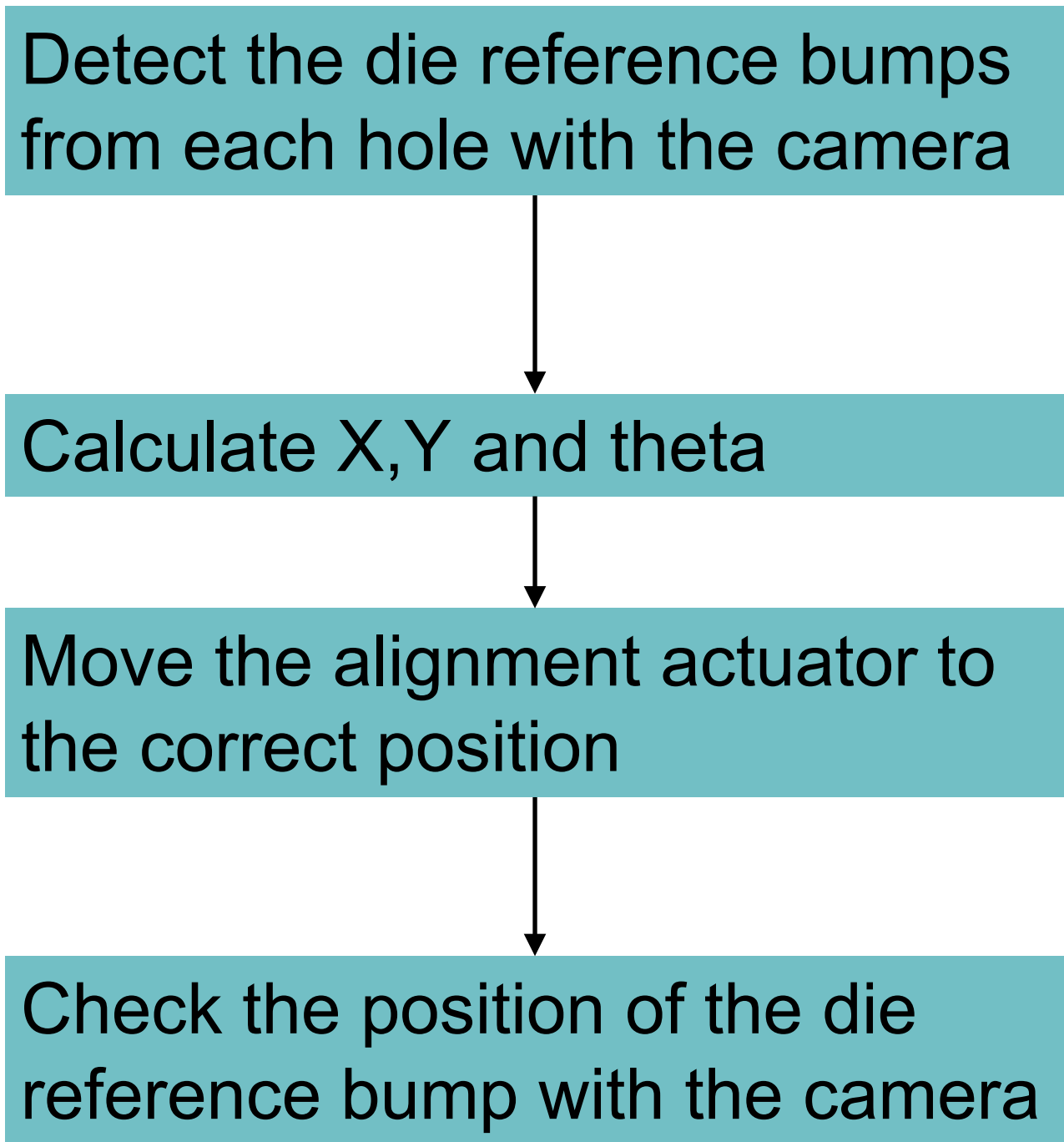
- **High Power Density in HBM Stacks:**
 - An HBM 3D memory stack die can dissipate significant power during test
 - In a high-parallel testing, the total heat load poses a serious thermal management challenge
- **Thermal control by memory handler**
 - Die temperature is well controlled by connecting memory handler
 - The handler has individual sensor and applies cooling air to keep die Tj

item	value
Parallelism	64
Heat generation	15W
temperature	105°C
Tj rise(all Die)	≤3°C



Alignment accuracy & repeatability

- **Automated alignment processes:**



Conclusion

- **Technical Advantage – Die-Level Testing**
 - Singulated die testing allows full-speed, multi-temperature screening before stacking
 - One-time contact via die carrier achieves complete test coverage (DC, functional, etc.) in a single insertion
 - Supports high parallelism, improving overall throughput without compromising test quality
- **Scalability and Future Applications**
 - The short transmission path of the die carrier architecture enables reliable multi-GHz test performance
 - Well suited for wafer-level high-speed memory testing and future chiplet architectures

Acknowledgement & Contact information

The authors express their gratitude to Abdelrahman Awad from FormFactor as well as Toshiyuki Kiyokawa and Atsushi Nakadate from Advantest for their valuable contribution to this paper.

Alan Liao
Asia Region Product Marketing Director
ALiao@formfactor.com

Hiromitsu Takasu
Device Interface Business Development Manager
hiromitsu.takasu@advantest.com